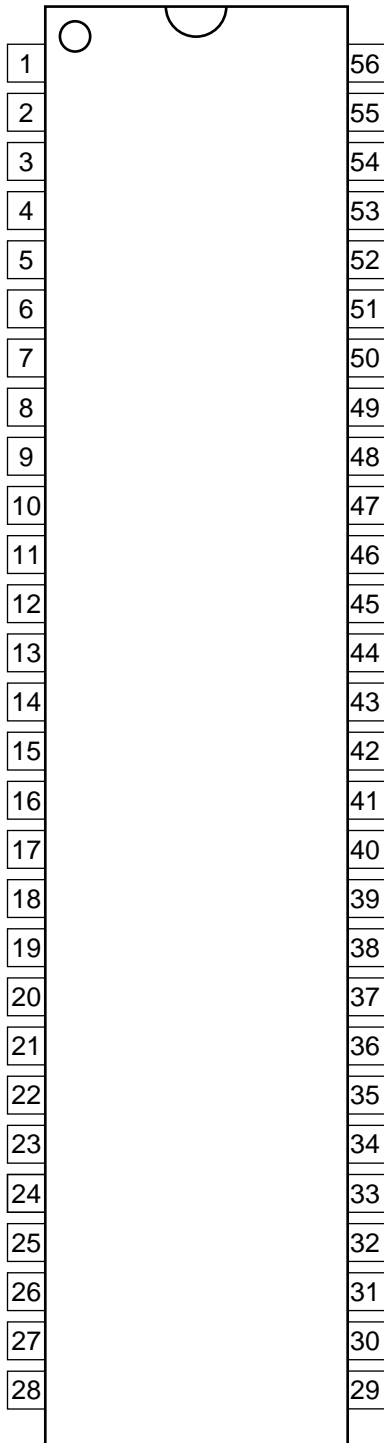


20-BIT D-TYPE FLIP-FLOP

—TOP VIEW—

**INPUTS**

CLK1, CLK2 : CLOCK

D0 - D19 : INPUT

 $\overline{OE}1, \overline{OE}2$: OUTPUT ENABLE**OUTPUTS**

O0 - O19 : OUTPUT

INPUTS			OUTPUTS
CLK1	$\overline{OE}1$	D0 - D9	O0 - O9
x	1	x	HI-Z
\uparrow	0	0	0
\uparrow	0	1	1
0 or 1	0	x	Q0

INPUTS			OUTPUTS
CLK2	$\overline{OE}2$	D10 - D19	O10 - O19
x	1	x	HI-Z
\uparrow	0	0	0
\uparrow	0	1	1
0 or 1	0	x	Q0

0 : LOW LEVEL

1 : HIGH LEVEL

x : DON'T CARE

HI-Z : HIGH IMPEDANCE

Q0 : PREVIOUS Q0 BEFORE LOW-TO-HIGH TRANSITION OF CLOCK

 \uparrow : LOW-TO-HIGH TRANSITION

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	I	$\overline{OE}1$	15	O	O10	29	I	CLK2	43	I	D9
2	O	O0	16	O	O11	30	I	D19	44	I	D8
3	O	O1	17	O	O12	31	I	D18	45	I	D7
4	—	GND	18	—	GND	32	—	GND	46	—	GND
5	O	O2	19	O	O13	33	I	D17	47	I	D6
6	O	O3	20	O	O14	34	I	D16	48	I	D5
7	—	Vcc	21	O	O15	35	—	Vcc	49	I	D4
8	O	O4	22	—	Vcc	36	I	D15	50	—	Vcc
9	O	O5	23	O	O16	37	I	D14	51	I	D3
10	O	O6	24	O	O17	38	I	D13	52	I	D2
11	—	GND	25	—	GND	39	—	GND	53	—	GND
12	O	O7	26	O	O18	40	I	D12	54	I	D1
13	O	O8	27	O	O19	41	I	D11	55	I	D0
14	O	O9	28	I	$\overline{OE}2$	42	I	D10	56	I	CLK1

